OIPE SC127
AUG 0 3 2001
PATENT & TRADEMARK OFFICE

2800 0420
8-3-01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
PATENT APPLICATION

2811

#3
D. Scott
2-7-02

Applicant: Shohhei Fujio and Hideki Kabayama — Art Unit: Unknown
Serial No.:09/682,131 — Examiner: Unknown
Filed: July 25, 2001 — Atty. Docket:JP9-2000-0229-US1
Title: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE WITH EMI PREVENTION STRUCTURE

RECEIVED
AUG 23 2001
2800 MAIL ROOM

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR 1.56, 1.97, 1.98

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Applicants submit herewith form PTO-1449, listing patents, publications, or other information of which they are aware which they believe may be material to patentability pursuant to 37 CFR 1.56(b), and in respect of which there may be a duty to disclose under 37 CFR 1.56(a), together with legible copies of the patents, publications, or other information listed

While the items submitted with this Information Disclosure Statement may be material to patentability pursuant to 37 CFR 1.56, in accordance with 37 CFR 1.97(h) it shall not be construed to be an admission that any patent, publication, or other information cited is "prior art" or is material to patentability for this invention unless specifically designated as such. In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other information material to patentability, as defined in 37 CFR 1.56(b), exists.

Respectfully submitted,

Date: 8/1/2001

By: RA Walsh

Robert A. Walsh, Reg. No. 26,516
IP Law Department
IBM Corp.
1000 River Street
Essex Junction, VT 05452
Tel.: 802-769-9521